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Design and Control of a Grid-connected Seven Level Inverter for Photovoltaic Applications

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***Abstract* - This paper presents the design and closed-loop current control of a grid connected seven-level, 3-phase diode-clamped multilevel inverter for Photovoltaic (PV) applications. The proposed closed loop current control technique is based on the voltage-oriented proportional integral (PI) controller theory. The modulation technique used is level-shifted-carrier sinusoidal pulse width modulation (SPWM). The gain values of PI controller were selected to achieve good current quality and dynamic response. Grid synchronization was achieved by using a synchronous-reference frame phase-locked loop (SRF-PLL). Matlab/Simulink was used for the control system design and simulation. The simulation results show that a 1.34% total harmonic distortion (THD) of the output current was achieved which is within the allowable current distortion limits by international standards. The stability of the system was analyzed using pole-zero mapping and root locus.**

Keywords: diode-clamped, level-shifted carrier, current control, stability

I. INTRODUCTION

Multi-level inverters convert direct current (DC) power to alternating current (AC) power at the required output voltage and frequency. With the high demand of electrical energy due to increasing industrial activities as a result of population growth, urbanization and the increased use of numerous electrical appliances there is need for clean, economical, and renewable energy to provide reliable power supply. Solar photovoltaic (PV) is one of the most promising and fastest growing renewable energy sources. Solar PV produces a DC voltage which has to be converted to AC for grid-integration. This is done using an inverter, the most common type of inverter being a two-level inverter. However, the implementation of two-level inverters is limited to low-power, low-voltage applications due to limitations in semiconductor device ratings, unless they are connected in series-parallel to increase their power handling capability. Series-parallel connection of semiconductor devices makes the inverter and control design more complicated.

Multi-level inverters provide an alternative method of grid-integration of PV power at higher power and voltage levels which are not possible with two-level inverters. Some advantages of multi-level inverters over two-level inverters are increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission [1]. Due to their higher voltage handling capability, multi-level inverters allow the connection of PV systems to the medium voltage grid, without the use of a transformer, which would have made the system more bulky, expensive and increase the power losses. The higher voltage handling capability is achieved with the use of lower voltage-rated devices, which is more economical than series-parallel connection of devices. [2].

The diode clamped multi-level inverter, is one of the most commonly used multilevel inverter topologies. Diodes are used as clamping devices to clamp the dc bus voltage so as to achieve "steps" in the output voltage. It also uses capacitors connected in series across the DC input voltage to divide the DC bus voltage into a set of voltage levels.

The performance of the diode clamped multilevel inverter is also determined by the modulation and control schemes used. The control scheme used in this paper is voltage-oriented PI control. This involves coordinate transformation of three-phase current into the synchronous reference frame, where AC currents appear as DC currents and PI controllers can be utilized without the inherent steady-state error which occurs when they are used with sinusoidal signals [3]. Various pulse-width modulation (PWM) schemes for multi-level inverters have been presented in literature. The carrier based pulse width modulation (PWM) schemes are classified into two categories, namely; phase-shifted carrier modulation and level-shifted carrier modulation [4]. The level-shifted carrier modulation produces a lower Total Harmonic Distortion (THD) in the output current compared to phase shifted carrier modulation when applied in grid connected applications. It is also more flexible and easier to implement than the phase-shifted carrier modulation. [5].

The grid filter is the other component which determines the performance of the inverter. The most common filter types are the first-order inductive (L) filter, second order capacitive-inductive (LC) filter and the third-order inductive-capacitive-inductive (LCL) filter. The LCL filter is suitable for high-power, medium voltage applications where the switching frequency is relatively low to reduce switching losses. It provides high attenuation of switching harmonics with relatively small filter components. A drawback of the LCL filter is resonance at its resonance frequency which affects the controller stability, unless a suitable control scheme is used [6].

This paper presents a closed-loop current control scheme for a seven-level three-phase diode-clamped dc–ac inverter using the level-shift carrier sinusoidal pulse width modulation (SPWM) based on voltage-oriented PI control. A synchronous-reference-frame phase-locked-loop is implemented for grid synchronization. Simulation results from Matlab/Simulink are presented to demonstrate the operation of the grid-connected seven level diode clamped multi-level inverter.

The paper is organised as follows: In section II, the overview of the grid-connected system is presented. In section

III, the details of the system design and modelling are given. In section IV, the stability analysis is presented. In section V, the simulation results are presented and section VI is the conclusion.

II. SYSTEM DESCRIPTION

To produce n-levels of the phase voltage, an n-level diode-clamped multilevel inverter needs $n-1$ capacitors on the DC bus. It also requires $2(n-1)$ main switches and $2(n-1)$ anti-parallel diodes on the main switches. The anti-parallel diodes are normally integrated into the main switch. The number of clamping diodes needed is $(n-1)(n-2)$ [7]. The voltage across each capacitor for an n-level diode clamped inverter in steady state is $V_{dc}/(n-1)$. Thus, each active switching device is only required to block a voltage of $V_{dc}/(n-1)$, where n is the number of levels.

The single line diagram for a Grid connected seven- level diode clamped multilevel inverter with a DC-Link is shown in Fig. 1.

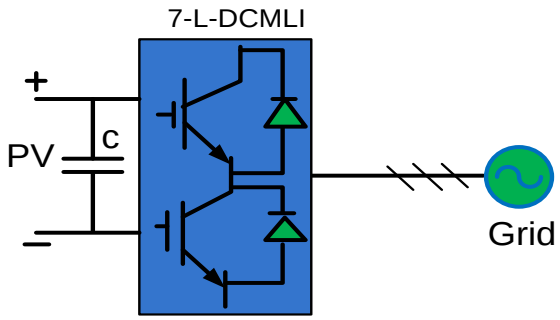

Fig.1: Single line diagram of a grid connected seven Level-DCMLI

The detailed circuit diagram of a seven-level diode-clamped multilevel inverter is shown in Fig. 2. For simplicity and ease of reference only one leg (phase) has been shown. The circuit consists of twelve (12) Insulated Gate Bipolar Transistors (IGBTs) with their anti-parallel diodes, thirty (30) clamping diodes and six (6) capacitors. This topology was proposed by Nabae, Takahashi, and Akagi in 1981 and it is one of the mostly used topology for grid connected photovoltaic systems [8].

The switching sequences of the 7 level diode clamped multilevel inverter is explained as follows:

Switching sequence 1:- In this switching status Q_1, Q_2, Q_3, Q_4, Q_5 and Q_6 are turned on and the output voltage across the load is $V_{dc}/2$.

Switching sequence 2:- In this switching status Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are tuned on and the output voltage across the load is equal to $V_{dc}/3$.

Switching sequence 3:- In this switching status Q_3, Q_4, Q_5, Q_6, Q_7 and Q_8 are turned on and the output voltage across the load is equal to $V_{dc}/6$.

Switching sequence 4:- In this switching status Q_4, Q_5, Q_6, Q_7, Q_8 and Q_9 are turned on and the output voltage across the load is zero.

Switching sequence 5:- In this switching status Q_5, Q_6, Q_7, Q_8, Q_9 and Q_{10} are turned on and the output voltage across the load is $-V_{dc}/6$.

Switching sequence 6:- In this switching status Q_6, Q_7, Q_8, Q_9, Q_{10} and Q_{11} are turned on and the output voltage across the load is $-V_{dc}/3$.

Switching sequence 7:- In this switching status Q_7, Q_8, Q_9, Q_{10}, Q_{11} and Q_{12} are turned on and the output voltage across the load is $-V_{dc}/2$.

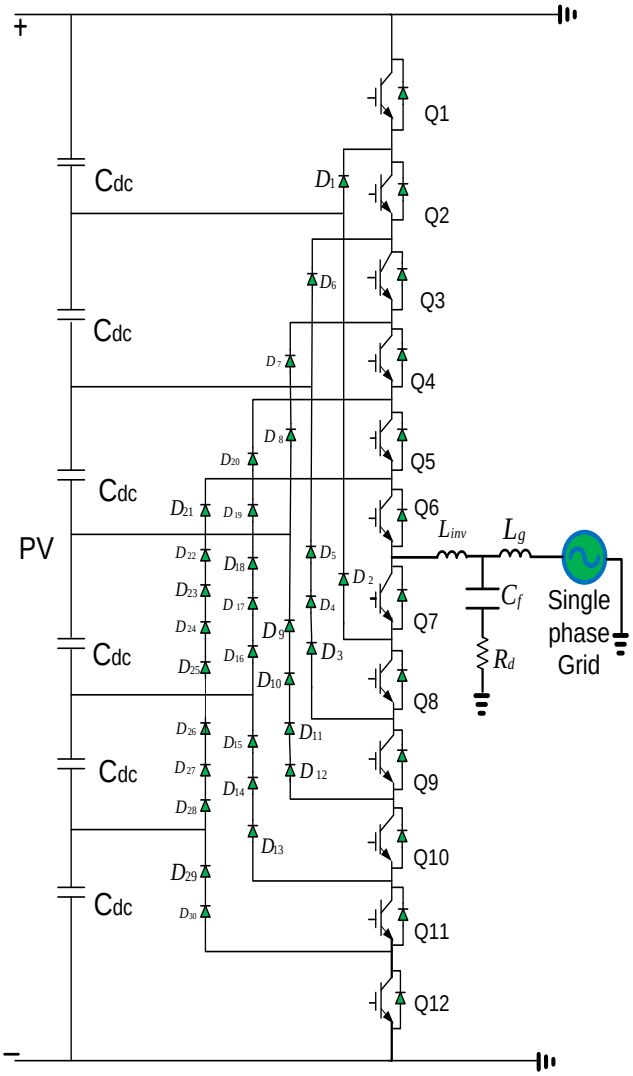

Fig. 2: Detailed circuit of a grid connected single phase seven- level diode clamped inverter

III. SYSTEM DESIGN AND MODELING

A. LCL Filter Design

Industrial LCL-based grid inverters are designed in view of robustness, stability and high efficiency. Several design methods are presented in [3], [9] and an improved design method including the stability and controllability of the system is discussed in [10]. The choice of sensor position for a grid connected inverter with an LCL filter depends on application, voltage and current level [11, 12]. The two possible positions are inverter-side and grid-side. An inverter-side current sensor is required for current measurement and protection [13] while for grid connected applications a grid-side voltage sensor is necessary for synchronisation [14, 15]. Some researches show that if the current sensors are on the grid side, rather than on the inverter side, the current control loop is much closer to stability [16]. The stability of the closed-loop control system can be improved by the addition of a passive damping or an active damping scheme [17]. The passive damping scheme is

more attractive than the active damping scheme due to its simplicity of implementation and lower cost [17].

The single phase equivalent circuit of the LCL filter with passive damping in of resistors connected in series with the filter capacitor is shown in Fig. 5 below. The equivalent resistances R_1 and R_2 are usually small and their resistance can be ignored.

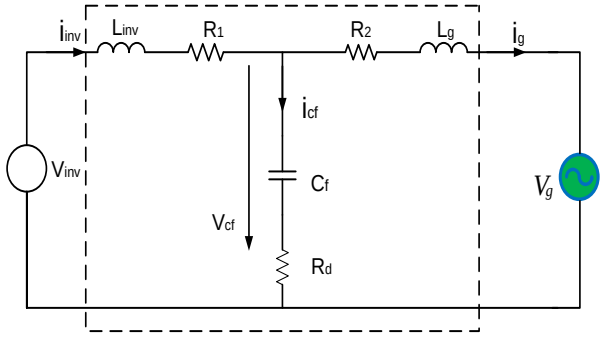

Fig. 3: The equivalent circuit of an LCL filter with a damping resistor

The time domain mathematical model of the system can be described using space vector notation.

The inverter voltage is related to the DC voltage by

$$\underline{v}_{inv}^{\,abc} = \underline{m}^{abc}\frac{v_{dc}}{2} \tag{1}$$

Where $\underline{v}_{inv}^{\,abc}$ is the inverter voltage space vector in the natural (abc) reference frame, $\underline{m}^{abc}$ is the modulation index in the natural reference frame, and v_{dc} is the DC voltage.

The inverter voltage is related to the filter capacitor voltage by

$$\underline{v}_{inv}^{\,abc} = \underline{v}_{Cf}^{\,abc} + L_1\frac{d\underline{i}_{L1}^{\,abc}}{dt} \tag{2}$$

Where $\underline{v}_{Cf}^{\,abc}$ is the filter capacitor voltage space vector in the natural reference frame, L_1 is the inverter side filter inductance and $\underline{i}_{L1}^{\,abc}$ is the inverter side current space vector in the natural reference frame.

The filter capacitor voltage is related to the grid voltage by

$$\underline{v}_{Cf}^{\,abc} = \underline{v}_{g}^{\,abc} + L_2\frac{d\underline{i}_{L2}^{\,abc}}{dt} \tag{3}$$

Where $\underline{v}_{g}^{\,abc}$ is the grid voltage space vector in the natural reference frame, L_2 is the grid side filter inductance and $\underline{i}_{L2}^{\,abc}$ is the grid side current space vector in the natural reference frame.

The currents are related by

$$\underline{i}_{L1}^{\,abc} = \underline{i}_{L2}^{\,abc} + \underline{i}_{Cf}^{\,abc} \tag{4}$$

Where $\underline{i}_{Cf}^{\,abc}$ is the filter capacitor current space vector in the natural reference frame.

The system transfer function model of LCL filter with a damping resistor is shown in Fig. 6 below with R_1 and R_2 ignored.

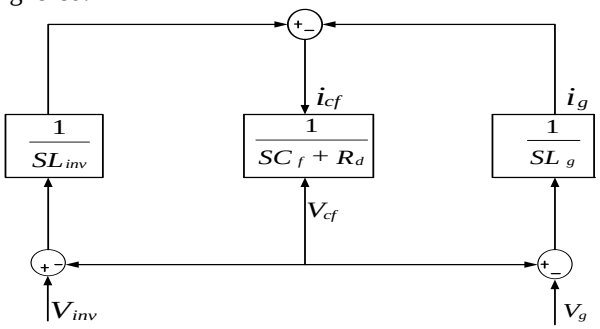

Fig. 4: Block diagram model of LCL filter with a damping.

The values of the filter components can be calculated using the procedure given in [15]. The base impedance is given by

$$Z_b = \frac{V_{grid}^{\,2}}{P_{rated}} \tag{5}$$

The base capacitance is given by

$$C_b = \frac{1}{\omega Z_b} \tag{6}$$

The filter capacitor is limited to 0.05 pu of the base capacitance to limit the reactive power consumption of the inverter. Therefore, the filter capacitor is given by

$$C_f \le 0.05C_b \tag{7}$$

The rated maximum current is given by

$$I_{\max} = \frac{\sqrt{2}P_{rated}}{\sqrt{3}V_{grid}} \tag{8}$$

The maximum allowable ripple in the inductor current is selected to be 10% of the maximum current and is given by

$$\Delta I_{\max} = 0.1I_{\max} \tag{9}$$

The inverter-side inductor should be designed such that it is capable of limiting the ripple in the inverter current to 10% of the rated amplitude value [18]. Thus, it is given by

$$L_1 = \frac{V_{dc}}{16\Delta I_{\max} f_{sw}} \tag{10}$$

The grid-side inductance is selected as a fraction of the inverter-side inductance and is given by

$$L_2 = rL_1 \tag{11}$$

Where r < 1.

The value of r in this work has been taken as 0.3.

The optimum value of damping resistor is selected using such that the damping factor, ζ, is 0.707 [19]. The damping factor is related to the damping resistor by

$$\zeta = \frac{C_f\omega_{res}R_d}{2} \tag{12}$$

Where ω_{res} is the resonance frequency of the LCL filter.

The resonance frequency of the LCL filter is very critical in the design and is given by

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{13}$$

Too high or too low values of resonance frequency of the LCL filter should be avoided. The resonance frequency of the LCL filter should better be 10 times greater than the grid frequency, and less than half of the switching frequency [17].

$$10 f_1 < f_{res} < 0.5 f_{sw} \tag{14}$$

Where f_1 is the fundamental frequency and f_{sw} is the switching frequency.

B. Grid Synchronization

The SRF-PLL has been implemented in this paper for grid synchronization due to its robustness in various grid conditions. It is easy to implement, it is effective, and it is reliable [20].

The major role played by the PLL is to provide Grid synchronization which is a very important function in grid connected inverters. The Phase Locked Loop (PLL) will detect the frequency and phase from the grid system, and the phase angle is used as the angle for coordinate transformation from abc to dq. The SRF-PLL has three major components namely; phase detector (PD), loop filter, and a voltage controlled oscillator (VCO) [21]. The block diagram of the SRF-PLL block diagram is shown in Fig. 5.

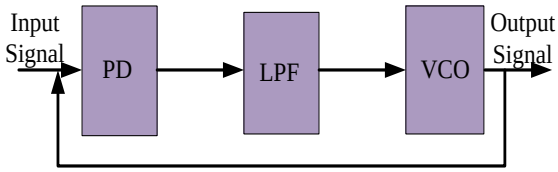

Fig. 5 Block diagram of Phase Locked Loop

C. Current Controller

The PI controller has been widely used as current controller in a variety of inverter applications. The design and implementation of this controller is simple, its algorithm has a low computational and it is stable, making it useful as a current controller in most inverter topologies [22], [23], [24]. The proportional integral (PI) current control technique is employed for grid connected PV inverters to keep the output current sinusoidal and to achieve high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity [25]. The transfer function for the PI controller is given by

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{15}$$

Where K_p is the proportional gain and K_i is the integral gain.

IV. STABILITY ANALYSIS

The system transfer function can be given by

$$G_{LCL}(s) = \frac{I_g(s)}{V_{inv}(s)} = \frac{R_d C_f s + 1}{L_1 L_2 C_f s^3 + (L_1 + L_2) R_d C_f s^2 + (L_1 + L_2) s} \tag{16}$$

If there is no damping resistor the transfer function is given by

$$G_{LCL}(s) = \frac{I_g(s)}{V_{inv}(s)} = \frac{1}{L_1 L_2 C_f s^3 + (L_1 + L_2) s} \tag{17}$$

The pole-zero map of the undamped LCL filter is shown in Fig. 6.

The filter has got three poles. One is at the origin, while two are imaginary poles lying on the imaginary axis. This indicates marginal system stability. Therefore, an undamped LCL filter is a marginally stable system and if it connected to the grid and the control system is added, it is likely to become unstable.

The pole-zero map of a damped LCL filter is shown in Fig. 7. The filter has a pole at the origin and two complex poles on the left-hand side of the imaginary axis. This indicates that the system is stable. If a stable LCL filter is connected to the grid, and a suitably tuned controller, it will remain stable.

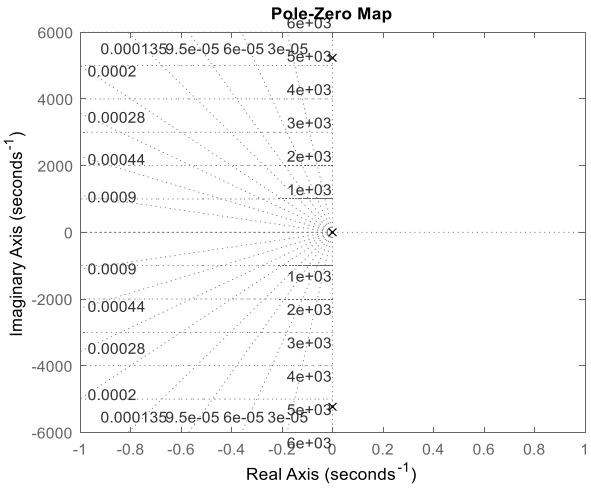

Fig. 6 Pole-zero map of undamped LCL filter

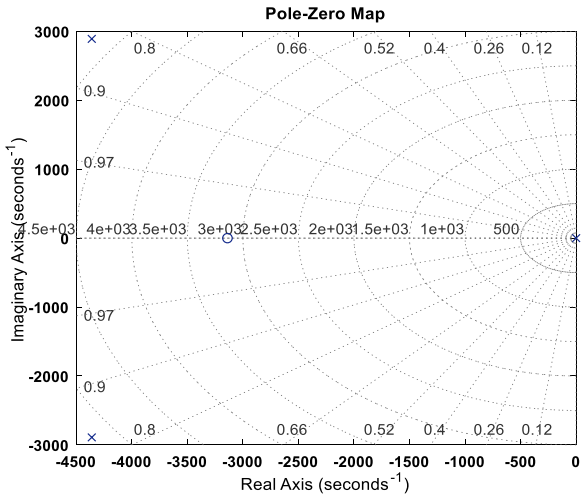

Fig. 7 Pole-zero map of damped LCL filter

The stability of the LCL filter for various values of controller gain is investigated using the root locus method.

The root locus of an undamped LCL filter is shown in Fig. 8. The root locus shows that increasing the controller gain causes the imaginary poles of the filter to move to the right of the imaginary axis as complex poles. Complex poles on the right hand side of the imaginary axis are an indication of undamped oscillations which cause the system to be unstable.

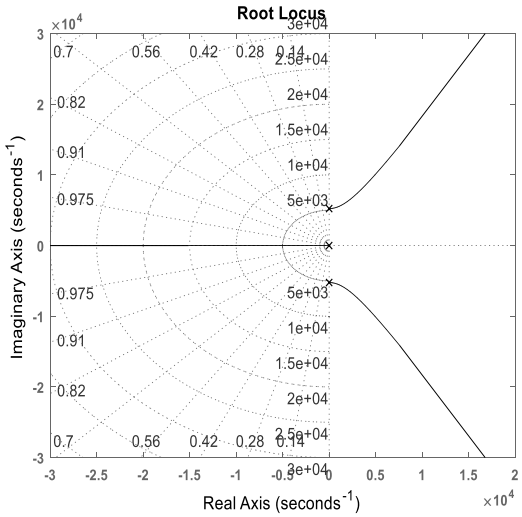

Fig. 8 Root locus of undmaped LCL filter

The root locus of a damped LCL filter is shown in Fig.9. The plot shows that the poles of the system remain on the left of the imaginary axis for all values of controller gain. This shows that the system is stable for all values of controller gain.

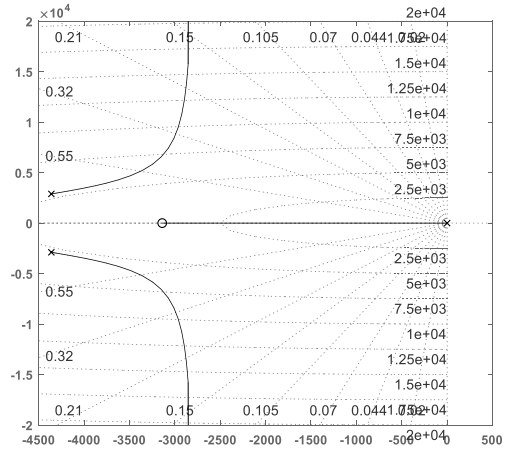

Fig. 9 Root locus of damped LCL filter

V. SIMULATION RESULTS

The parameters of the system being considered are shown in Table. 1.

TABLE 1 Parameters of the simulation model

Parameter	**Value**
Rated Power, P_{rated}	2 MW
DC voltage, V_{dc}	6 kV
Grid voltage, V_g	3.3 kV
Grid frequency, f_g	50 Hz
Switching frequency, f_{sw}	2 kHz
Grid side inductance, L_2	1.5 mH
Inverter side inductance, L_1	7.5 mH
Damping resistance, R_d	10.9 Ω
Filter capacitor, C_f	29.23 µF

The block diagram of the grid-connected inverter and its control scheme is shown in Fig. 10.

The inverter output voltage waveform for phase-a is shown in Fig. 11. The waveform is a stair-case waveform with seven levels as expected from a seven-level inverter. The stair case waveform reduces the filtering requirements on the inverter output, and reduces the distortion in the current.

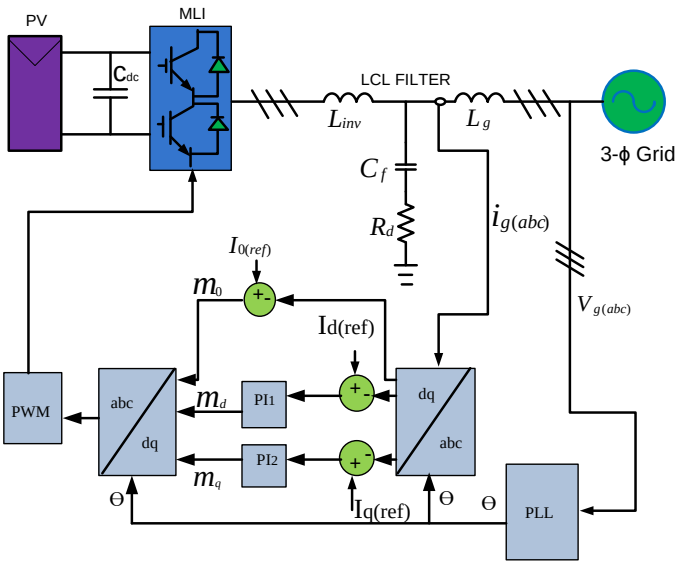

Fig. 10 Block diagram of grid-connected inverter and control scheme

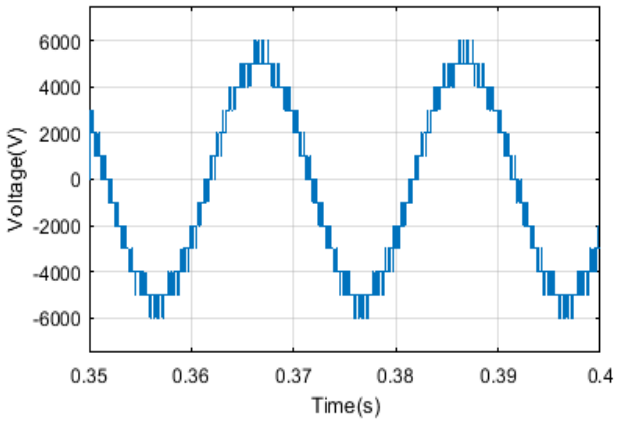

Fig. 11 Output voltage waveform for one phase

The waveform of the steady-state grid current is shown in Fig.12. The frequency spectrum of the current is shown in Fig. 13. The frequency spectrum shows that the total harmonic distortion (THD) of the current is 1.34 %, which is much lower than the maximum allowable THD of 5 %.

The dynamic performance of the system is shown in Fig. 14 and Fig. 15. In Fig.14, the response of the d-axis current to a step change of 1 p.u. in current is shown. The response is fast and accurate, showing that the PI controller is well tuned to achieve good dynamic performance and good steady-state

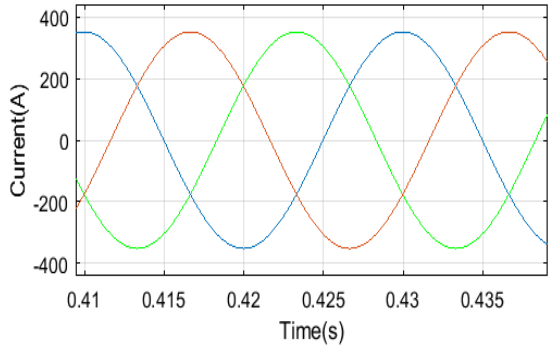

Fig. 12 Steady-state grid current waveforms

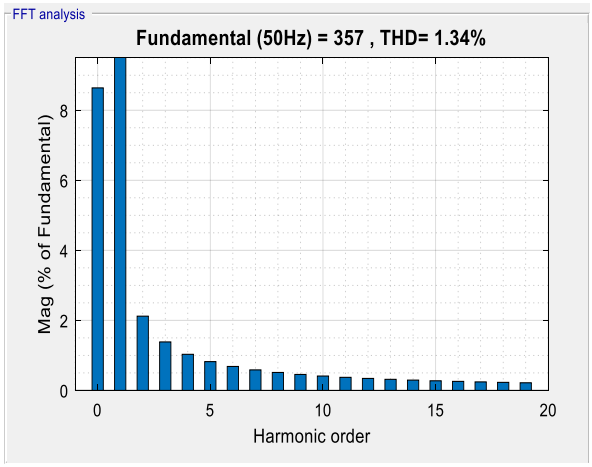

Fig. 13 Frequency spectrum of grid current

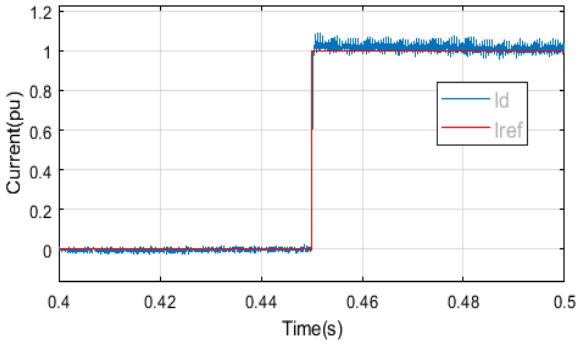

Fig. 14 Measured and reference d-current

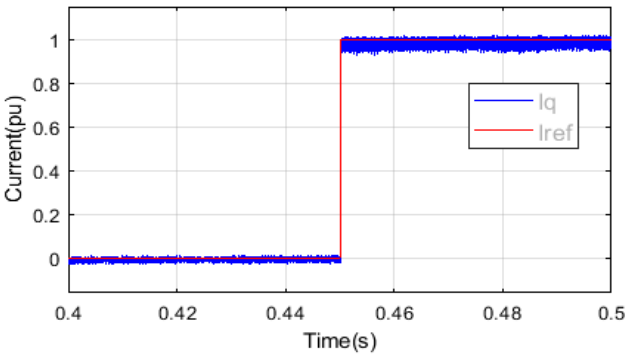

Fig. 15 Measured and reference q-axis current

tracking with zero steady-state error. Fig. 15 shows a similar performance for the q-axis current.

VII. CONCLUSION

The grid-connected seven-level inverter with an LCL filter has been successfully designed and implemented in Matlab/Simulink. The LCL filter is designed to achieve stability using a simple passive damping resistor. Stability is achieved for all values of controller gain. The simulation results show good steady-state performance and a THD of 1.34 % in the grid current is achieved. The results also show good dynamic performance demonstrated by the response of the current to a step change in the reference current. The measured current follows the reference current showing a fast dynamic response. A steady-state error of zero is achieved due to the controller being implemented in the synchronous reference frame. In future, the design and control scheme

resented in this paper will be applied to a practical prototype to validate the simulation results.

REFERENCES

[1] N.Das Jaya Raj, P. Bala Krishna and K. Manoz Kumar Reddy, "Analysis of Different Multilevel Converter Topologies for Photovoltaic Applications", International Journal for Modern Trends in Science and Technology, Volume: 03, Issue No: 09, September 2017.

[2] Sergio Busquets-Monge, José Daniel Ortega, Josep Bordonau, José Antonio Beristáin, and Joan Rocabert, "Closed-Loop Control of a Three-Phase Neutral-Point- Clamped Inverter Using an Optimized Virtual-Vector-Based Pulse width Modulation". IEEE Transactions on Industrial Electronics, VOL. 55, No. 5, May 2008.

[3] Jeyraj Selvaraj and Nasrudin A. Rahim, "Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller", IEEE Transactions on Industrial Electronics, Vol. 56, No. 1, January 2009.

[4] M. Sudhakaran and R. Seyezhai "A Review of Various Carrier Pwm Techniques for Trinary Cascaded Multilevel Inverter" Middle-East J. Sci. Res., 24 (Recent Innovations in Engineering, Technology, Management & Applications): 81-89, 2016.

[5] Mohit Jain et al. Comparative Analysis and Simulation of Diode Clamped & Cascaded H-Bridge Multilevel Inverter using SPWM Technique". International Journal of Engineering Research and Applications, Vol. 5, Issue 1(Part5), January 2015, pp.95-102.

[6] Y. Tang, S. Member, P. C. Loh, P. Wang, and F. H. Choo, "Generalized Design of High Performance Shunt Active Power Filter With Output LCL Filter," IEEE Transactions on Industrial Electronics, vol. 59, no. 3, pp. 1443–1452, 2012.

[7] Leon M. Tolbert, Fang Zheng Peng, and Thomas G. Habetler, "Multilevel Converters for Large Electric Drives," IEEE Transactions on Industry Applications, Vol. 35, No. 1, January/February 1999.

[8] Bimal K. Bose, "Multi-Level Converters". Electronics 2015, 4, 582-585.

[9] E. Kantar, "Design and control of PWM converter with LCL type filter for grid interface of renewable energy systems" Master Thesis, 2014.

[10] Dannehl, J., Liserre, M., Fuchs, F.W. "Filter based active damping of voltage source converters with LCL filter", IEEE Trans. Ind. Electron., 2011, 58, (8), pp. 3623–3633.

[11] Dannehl, J., Fuchs, F.W., Hansen, S., Thgersen, P.B.: "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," IEEE Trans. Ind. Appl., 2010, 46, (4), pp. 1509–1517.

[12] Pena-Alzola, R., Liserre, M., Blaabjerg, F., Yang, Y.: "Robust design of LCL-filters for active damping in grid converters," IECON 2013–39th Annual Conf. IEEE Industrial Electronics Society, pp. 1248–1253.

[13] Tsili, M., Papathanassiou, S. "A review of grid code technical requirements for wind farms," IET Renew. Power Gener., 2009, 3, (3), pp. 308–332.

[14] Xie, D., Xu, Z., Yang, L., et al. "A comprehensive LVRT control strategy for DFIG wind turbines with enhanced reactive power support," IEEE Trans. Power Syst., 2013, 28, (3), pp. 3302–3310.

[15] Remus Teodorescu, Frede Blaabjerg and Marco Liserre and Antonio Dell'Aquila, "A stable three-phase LCL-filter based active rectifier without damping," IEEE, 2003.

[16] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," IEEE Trans. Power Electron., vol. 21, no. 1, pp. 263–272, Jan. 2006)

[17] Shen Guoqiao, Xu Dehong, Xi Danji, et al. "An improved control strategy for grid-connected voltage source inverters with a LCL filter", IEEE 21th Annual, pp.1067-1073, 2006.

[18] Noah K. Serem, "Electrical Power Quality Improvement for Renewable Energy Systems Using LCL Filter," International Journal of Scientific & Engineering Research, Volume 6, Issue 10, October-2015 954 ISSN 2229-5518.

[19] R. W. Erickson, D. Maksimovic, "Fundamentals of Power Electronics", Second Edition, Kluwer Academic Publishers, 2001.

[20] Samuel Vasconcelos Araújo, Alfred Engler, Benjamin Sahan, and Fernando Luiz Marcelo Antunes, "LCL Filter design for grid-connected NPC inverters in offshore wind turbines", *The 7th International Conference on Power Electronics, October 22-26, 2007.*

[21] Mostafa Ahmadzadeh, Saeedollah Mortazavi and Mohsen Saniei, "Applying the Taguchi Method for Investigating the Phase-Locked Loop Dynamics Affected by Hybrid Storage System Parameters", Energies 2018, 11, 226; doi:10.3390/en11010226.

[22] Golestan, S.; Monfared, M.; Freijedo, F.D.; Guerrero, J.M. Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems. IEEE Trans. Power Electron. 2012, 27, 3639–3650.

[23] K. Smriti Rao and Ravi Mishra, Comparative study of P, PI and PID controller for speed control of VSI-fed induction motor". International Journal of Engineering Development and Research, Volume 2, Issue 2, 2014.

[24] Bouzid, A.M.; Guerrero, J.M.; Cheriti, A.; Bouhamida, M.; Sicard, P.; Benghanem, M. A survey on control of electric power distributed generation systems for microgrid applications. Renew. Sustain. Energy Rev. 2015,44, 751–766.

[25] Ngoc Bao Lai and Kyeong-Hwa Kim, "An Improved Current Control Strategy for a Grid-Connected Inverter under Distorted Grid Conditions". Energies 2016, 9, 190; doi:10.3390/en9030190.